

Title: Ternary Digital System: Concepts and Applications

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Sequential Logic Design

INTRODUCTION

A sequential circuit is defined from the behavioral point of view as a circuit whose output depends on the present input as well as the past history of input or can be defined from the constructional point of view as a circuit that contains memory element. Figure 6.1 shows basic sequential circuit.

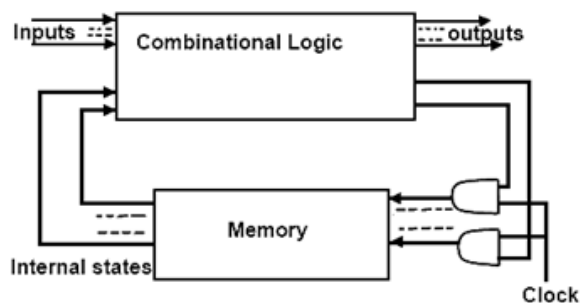


Figure 6.1: Diagram of sequential circuit.

Sequential circuit consists of combinational circuit and memory element in the feedback path of it. It has one input applied externally and one from memory element. An output is decided by external input signal and input from memory element.

A memory element is a medium in which one trit of information (0-2) can be stored and retained till needed and there after it's contain can be replaced by new value. The contain of circuit shown in Figure 6.1 can be changed by the output of combinational circuits that are concern to its input along with memory element. Above process demonstrates the dependence of external output of a sequential circuit on the external input and the new contains of memory element.

The sequential circuits are be classified in to two main categories viz Asynchronous and Synchronous circuits. Sequential circuit whose behavior depends upon the sequence in which the input signal changes is referred to as asynchronous and a sequential circuit whose behavior can be defined from the knowledge of its signal at discrete instance of time is referred to as synchronous circuits. The synchronization is achieved by a timing device known as system clock that generates a periodic train of clock pulses. The output is affected only with the application of clock pulses.

Ternary clock pulse is shown in Figure 6.2 below.

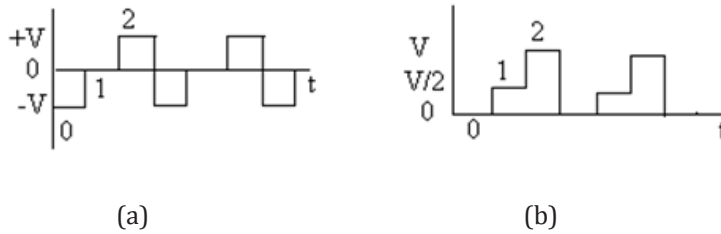


Figure 6.2: Ternary clock (a) Balance ternary clock (b) Unbalance ternary clock.

ONE TRIT MEMORY CELL

Ternary memory element is medium in which one trit of information is stored or retained till necessary, and thereafter its contents are replaced by new one. Basic ternary memory element is Flip-flap-Flop. It has three stable states 0-2. Figure 6.3 shows the basic ternary cell.

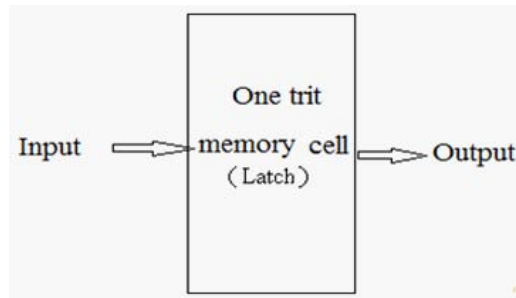


Figure 6.3: 1-trit memory element.

Latch: It is a circuit in which it is possible to latch (lock) and retrieve (open) the information as and when required. The circuit for latch is shown in Figure 6.4(a)

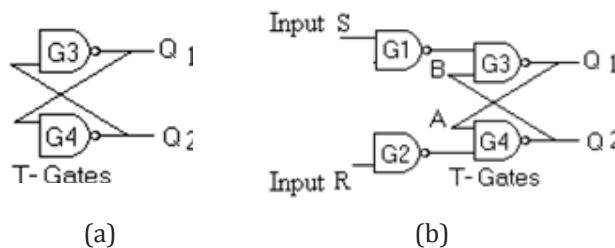


Figure 6.4 (a): 1-trit memory (b): 1-trit latch with input gates.

Basic ternary digital memory circuit is known as flip-flap-flop. It has three states i.e. 0, 1 and 2. It can be obtained by using NAND gates. Outputs Q_1 and Q_2 will depend on power On condition. Assume that initially $Q_1 = 0$ then $Q_2 = 2$, When $Q_1 = 1$, Q_2 will also be 1 and for $Q_1 = 2$, Q_2 will be 0 thus maintaining flip-flap-flop condition. There is no provision to store desired inputs. It is possible by

adding gates with 1-trit memorycell as shown in Figure 6.4(b).

Assuming S,R,Q and Q_{n+1} as inputs and present and netx state output. Truth table for the same is shown in Table 6.1.

Table 6.1: SR flip -flap- flop.

S	R	Q	Q_{n+1}
0	0	0	0
0	1	1	0
0	2	2	0
1	0	0	1
1	1	1	1
1	2	2	1
2	0	0	2
2	1	1	2
2	2	2	2

As a way to compose ternary flip-flap-flop, the similar structure of Flip-Flops as in binary is applied. The fundamental flip-flops in binary logic are designed using NAND/NOR binary gates. Therefore by replacing binary gates by ternary gates it is possible to construct ternary Flip-flap-Flops. Figure 6.5 shows structure of R-S flip-flap-flop and its truth table is given in Table 6.2.

Table 6.2: Truth table for R-S FF

Clock	S	R	Q	Q_{n+1}
0	0	0	0	2
0	0	1	0	2
0	0	2	0	2
1	1	0	1	1
1	1	1	1	1
1	1	2	1	1
2	2	0	2	0
2	2	1	2	0
2	2	2	2	0

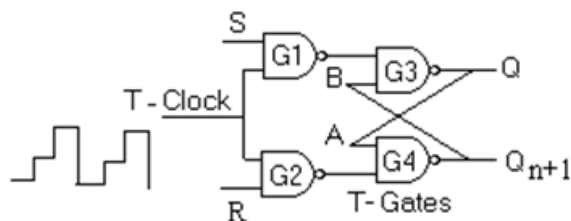


Figure 6.5: Structure of R-S flip-flap-flop

Assuming initially clock =0, R=2, S=0 & Q=0, here output of G1 is 2 & G2 is 0. Output of G4 will be 2 which is applied to G3, so the output of G3=0. Thus Q follows the clock pulses.

On the basis of R-S Flip-Flop, clock synchronized D-type flip-flop is constructed. The circuit for D-latch is shown in Figure 6.6. It has only one input referred to as D input. Its truth table is given in Table 8.3, from which it is clear that output Q_{n+1} at the end of clock pulse equals to input before the clock pulse. Symbols for T-S-R and D flip-flap-flop are as shown below in Figure 6.6 (a) and (b) respectively.

Table 6.2: Truth table for D flip flap flop

Input Dn	Output Dn+1
0	0
1	1
2	2

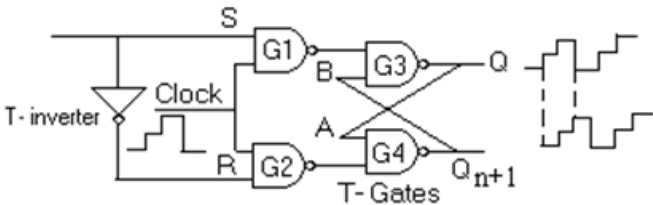


Figure 6.5: Structure of D-flip-flap-flop using S-R flip-flap-flop.

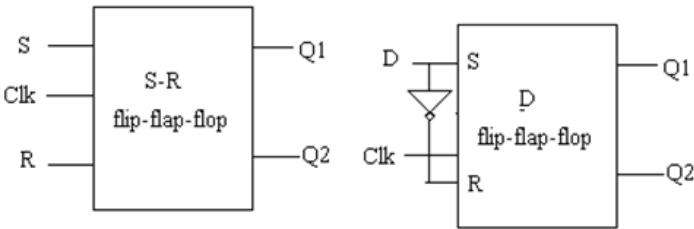


Figure 6.6: Block diagram for (a) S-R and (b) D flip-flap-flop.

APPLICATIONS OF SEQUENTIAL CIRCUITS

As an application of D-FFF ternary encoder is proposed [1]. As a means of data communication, ternary codes are preferred because of its information carrying capacity is much higher than binary [2]. Assume, message block as 11201(=k) in ternary code. The encoder generates message block of size n ($k < n$). Figure 6.7 shows ternary encoder. Here D1, D2 & D3 are ternary flip-flops. For the generation of codes assume all the flip-flops are cleared initially. During message bit interval commutator samples the modulo-3 adder outputs C_1 , C_2 & C_3 that is given by the equation.

$$C_1 = D_1 \oplus D_2 \oplus D_3$$

$$C_2 = D_1$$

$$C_3 = D1 \oplus D2$$

Thus single message bit gives three output bits. The next message bit in the input sequence enters the D1 and contents of D1 are shifted to D2. Commutators again sample the output during next bit interval. The process is repeated until last digit shifted to D3. The sequence of code generated by encoder is shown in Figure 6.7

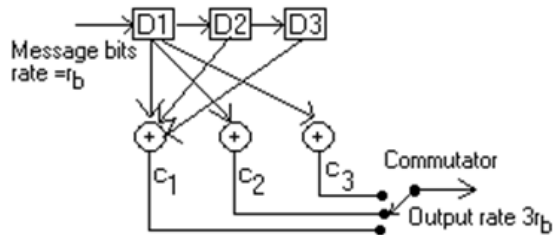


Figure 6.7: Ternary encoder.

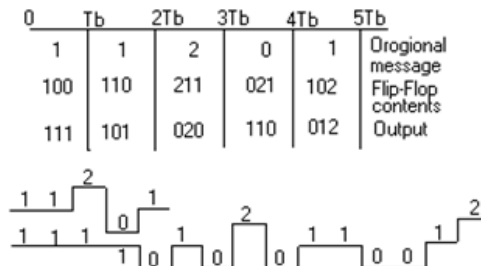


Figure 6.8: Encoding operation.

TERNARY COUNTERS

Ternary counter is a circuit that counts the number of pulses connected to it. T-flip-flap-flops are used to construct ternary counters. Figure 6.9 shows block diagram for T-flip-flap-flop with truth table. Two trit counter circuit is shown in Figure 6.10 along with counting pulses. Corresponding table is shown in Table 6.3 for two trit counter.

Input T	Output
0	Flip (0)
1	Flap (1)
2	Flop (2)

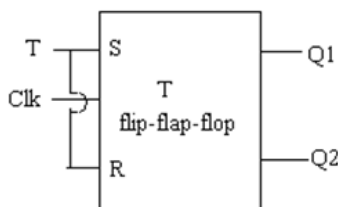


Figure 6.9: Block diagram for T-flip-flap-flop with truth table.

Table 6.3: Two trit counter.

Q0	Q1	Counting state
0	0	0
0	1	1
0	2	2
1	0	3
1	1	4
1	2	5
2	0	6
2	1	7
2	2	8

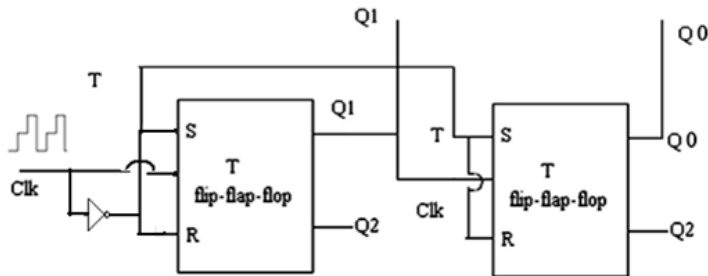


Figure 6.10: 2-trit counter.

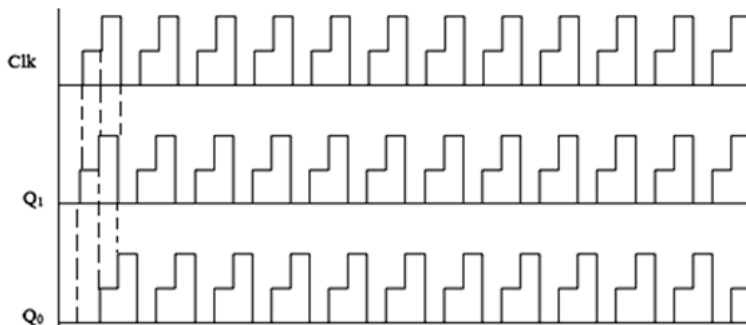


Figure 6.11: 2-trit counter waveform.

Figure 6.10 is a diagram for 2-trit counter and 6.11 shows corresponding counting pulses. When the clock is applied, initially Q0 and Q1 both stores o values. As the clock progresses, data in flip-flap-flop changes according to the rising edge of pulse. When clock changes from 0 to 1, data in Q1 is shifted to Q0 and new clock data is stored to Q1. The same sequence is followed by the clock pulse. Same analogy can be extended for design 'n' trit counter. An inverted clock has to connect to T input so that it will follow flip-flap-flop condition.

TERNARY SHIFT REGISTER

Difference between register and counter is, counters are use to counting number of digital

pulses connected to it whereas registers are use to store digital data according to clock pulse connected to it. This data is inputted through D- input of D-flip-flop-flop. Diagram for 2-trit register is shown in Figure 6.12. Registers are classified depending upon the way in which data are entered and retrieved. There are four possible modes of operation as below.

- 1) Serial in serial out.
- 2) Serial in parallel out
- 3) Parallel in serial out
- 4) Parallel in parallel out.

Figure 6.12 represent serial in serial out register. Remaining registers can be developing for other modes of operation.

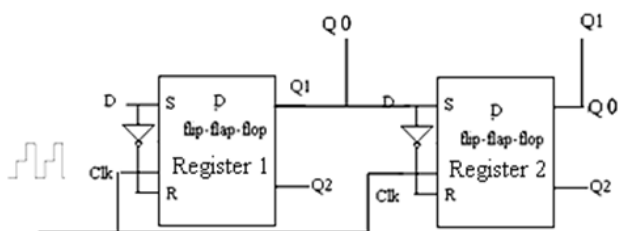


Figure 6.12: 2-trit serial in –serial out shift register.

Assume initially input D is 0 and clock pulse is applied, output from Q0 will be 0. After rising edge of pulse, Data from register 1 will be shifted to register 2 and flip-flap-flop will have new data in it. Assume again that data is now 1, then register 1 will have value 1 and output Q0 will be 1, in next cycle data2 will be shifted to register 1 and output Q0 will be 2 and so on. Below waveform indicates data flow sequence.

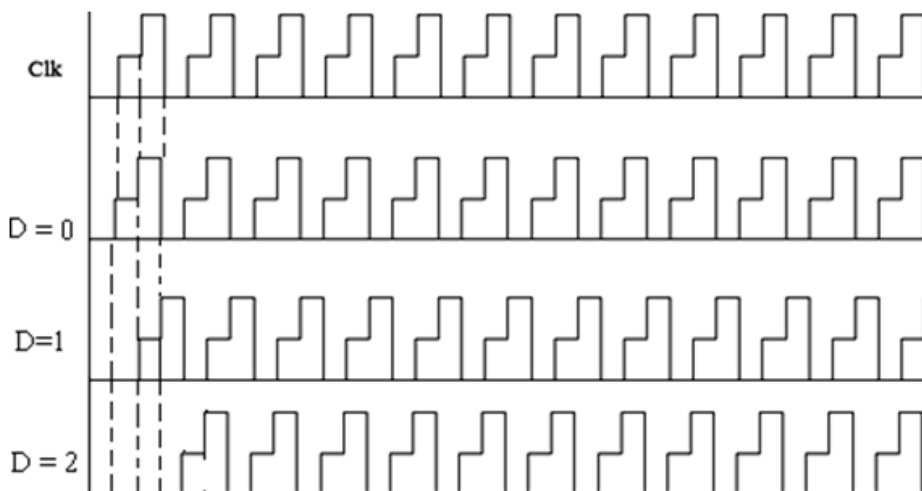


Figure 6.13: Data representation of serial in-serial out register.

References

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